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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/251,172	02/17/1999	AMMAR DERRAA	MI30-034	2938

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EXAMINER	
DONG, DALEI	

ART UNIT	PAPER NUMBER
2879	

DATE MAILED: 10/28/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/251,172	DERRAA, AMMAR	
	Examiner	Art Unit	
	Dalei Dong	2879	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 August 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *65-75* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *65-75* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of Claims 65-75 in the reply filed on August 12, 2004 is acknowledged.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 65-75 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,872,019 to Lee in view of U.S. Patent No. 5,655,940 and in further view of U.S. Patent No. 4,808,983 to Benjamin.

Regarding to claim 65, Lee discloses in Figure 3, a process for forming a base plate for a field emission display comprising providing a substrate configurable into a monolithic base plate (30) for the field emission display; forming a plurality of emitter regions (33) using the monolithic semiconductive substrate (see column 4, lines 29-42).

However, Lee does not disclose providing a luminescent member spaced from and opposite the monolithic semiconductive substrate; electrically isolating the plurality of emitter regions from one another; providing a plurality of emitters within individual ones of the emitter regions; providing a plurality of address circuits for respective ones of

the emitter regions and individually comprising row circuitry and column circuitry; coupling individual ones of the address circuits with emitters of respective individual ones of the emitter regions; using the respective address circuits, providing an electrical potential across selected ones of the emitters of the respective emitter regions; and responsive to the electrical potential, emitting electrons from the selected emitters towards the luminescent member to generate an image.

Hodson teaches in Figure 1, providing a luminescent member (24) spaced from and opposite the base plate (18); Hodson also teaches in Figure 2, electrically isolating the plurality of emitters regions (50, 60, 70 and 80) from each other; providing a plurality of emitter (14 shown in Figure 1) within individual ones of the emitter regions (see column 4, lines 7-11); providing a plurality of address circuits for respective ones of the emitter regions (50, 60, 70 and 80) and individually comprising row circuitry (100, 110, 120 and 125) and column circuitry (130, 140, 150 and 160); coupling individual ones of the address circuits with emitters of respective individual ones of the emitter regions (see column 4, lines 14-23); using the respective address circuits, providing an electrical potential across selected ones of the emitters of the respective emitter regions (see column 3, lines 50-56); and responsive tot eh electrical potential emitting electrons from the selected emitters toward the luminescent member to generate an image (see column 4, lines 37-42).

Benjamin teaches in Figure 13, there are two separately demarcated regions of pixels achieved by forming address rows that are effectively contained within the respective demarcated regions such that less than all (one half) of the pixel of a given row

are addressed by a single row address line. As evidenced by Benjamin, there are many applications for a monolithic display which lower RC time constant would allow for or improve the quality of the display.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have utilize the respective individual row and column circuitry to address the monolithic semiconductive substrate with plurality of emitters of Lee as taught by Benjamin to provide separate display regions each having independent driver means to increase the refresh rate for the monolithic display of appreciable size.

Regarding to claim 66, Hodson teaches the providing the electrical potential comprises applying the electrical potential across different elevational portion of the selected emitters of the respective emitter regions (see column 4, lines 43-51).

Regarding to claim 67, Hodson teaches passing the electrons through the vacuum towards the luminescent member (24) after the emitting (see column 3, lines 50-65); further it is old and well known in the art to provide a vacuum intermediate the monolithic semiconductive substrate and the luminescent member in order to facilitate the movement of the electrons.

Regarding to claim 68, Lee discloses in Figure 3, the electrically isolating comprises etching the monolithic semiconductive substrate to define the emitter regions (see column 4, lines 59-63).

Regarding to claim 69, Lee discloses in Figure 3, providing the emitters (33) comprises forming the plurality of emitter (33) to comprise bulk substrate material of the monolithic semiconductive substrate (see column 4, lines 59-63 also shown in Figures 1E and 5E).

Regarding to claim 70, Hodson teaches in Figure 1, the luminescent member (24) comprises a face plate (10).

Regarding to claim 71, Hodson teaches in Figure 1, the luminescent member comprises a phosphor material configured to generate the image responsive to the reception of the electrons (see column 3, lines 39-45).

Regarding to claim 72, Hodson teaches in Figure 2, the address circuit are individually configured to address the emitters of individual ones of the respective emitter regions independent of others of the address circuits (see column 4, lines 14-23).

Regarding to claim 73, Lee discloses in Figure 3, the emitters comprises etching bulk semiconductor material of the monolithic semiconductive substrate (see column 4, lines 59-63).

Regarding to claim 74, Hodson teaches in Figure 2, the row circuitry (100, 110, 120 and 125) and the column circuitry (130, 140, 150 and 160) of an individual one of

the address circuits comprises a plurality of address lines arranged orthogonal with respect to one another within the respective one of the emitter regions (also shown in Figure 7 of Lee reference).

Regarding to claim 75, Hodson teaches in Figure 2, the coupling of the address circuits with the emitters of the respective emitter regions comprises configuring individual ones of the address circuits to address the emitters of the respective emitter regions independent of addressing of the emitters of others of the emitter regions using others of the address circuits (see column 4, lines 14-23).

Response to Arguments

4. Applicant's arguments filed May 10, 2004 have been fully considered but they are not persuasive.

In response to Applicant's argument that Lee reference fails to teach or suggest plural emitter regions in combination with the monolithic semiconductive substrate; Examiner asserts that Lee discloses an "emitter region" of two emitters (33) in Figure 3, and Lee further discloses in Figure 7, that there are plurality of "emitter regions" that are addressed by column and row. Thus, Examiner asserts that the Lee reference discloses the claimed invention and maintains the rejection.

Also, in response to Applicant's arugment that Benjamin reference is related to liquid crystal display technology and is entirely irrelevant to the emitter teachings of the Lee reference or Hodson reference; Examiner asserts that Benjamin reference is used to

demonstrate that the reason to combine the Lee reference and Hodson reference is to providing separate display regions each having independent driver means to increase the refresh rate is not limited to tiled displays but includes monolithic display such as taught by the Lee reference, thus Examiner asserts that the Benjamin reference is valid and maintains the rejection.

Finally, in response to Applicant's argument that Hodson teaches using a plurality of discrete plates to form the display; Examiner asserts that Benjamin reference teaches there are many applications for a monolithic display which would allow for lower refresh time and thus improve the quality of the display. Therefore, the teachings of Hodson reference of providing independent means to address separate regions of the emitter to increase the refresh rate is clearly applicable to Lee reference because the monolithic display of Lee reference clearly has utility in video and other applications requiring a faster refresh rate than previously possible with monolithic displays of appreciable size. Thus, Examiner asserts that Hodson reference teaches the claimed invention and maintains the rejection.

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

The following prior art are cited to further show the state of the art of composition of a field emission display.

U.S. Patent No. 5,688,708 to Kato.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dalei Dong whose telephone number is (571)272-2370. The examiner can normally be reached on 8 A.M. to 5 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nimeshkumar Patel can be reached on (571)272-2457. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

D.D.
October 19, 2004

Joseph Williams
Primary Examiner
Art Unit 2879